Please amend the specification (all paragraphs) as follows:

METHOD OF MANUFACTURING FLASH MEMORIES OF ~~A~~ SEMICONDUCTOR DEVICES

BACKGROUND ~~OF THE INVENTION~~

Technical Field ~~of the Invention~~

~~The present invention relates to a method of manufacturing a semiconductor device, and more particularly, to a~~ A method of manufacturing ~~a~~ semiconductor devices is disclosed which can inhibit ~~prohibit generation of a~~ TED (transient enhanced diffusion) ~~phenomenon~~ of ~~a~~ dopant implanted into the bottom structure and which can also limit ~~prevent~~ degradation of the oxide film quality at the upper side due to outgasing~~,~~ that can occur during ~~in a subsequent~~ the annealing ~~process~~ after ~~an~~ the ion implantation ~~process~~ is implemented.

Discussion ~~Background~~ of the Related Art

In ~~order to~~ the manufacture ~~the~~ of semiconductor devices, ~~it is required that the~~ ion implantation processes, ~~as well as the~~ deposition processes and ~~the~~ etching processes are all used ~~be necessarily implemented~~.

In ~~general, in order to~~ the manufacture ~~the~~ flash memory devices or ~~the~~ transistors, a well region is formed by means of ~~the~~ an ion implantation process. An ion implantation layer for controlling the threshold voltage is then formed at a given depth of the well. Next, before a pad nitride film is formed, a tunnel oxide film and a first polysilicon layer for forming a floating gate is formed and is then patterned.

Thereafter, ~~a semiconductor substrate between the first polysilicon layers~~ the structure is etched to form a trench. A wall sacrificial oxidation process and a well oxidation process are then sequentially implemented to form an isolation film by

means of a SA-STI (self-aligned shallow trench isolation) method for electrically isolating the devices.

In the above process, in case of a ~~date~~ flash memory device using an nMOS transistor as a cell, boron (B) is implanted to form an ion implantation layer for adjusting the threshold voltage. At this time, as the cell is programmed and erased in a sector program/erase mode of 512 byte unit ~~in~~ of the ~~date~~ flash device, ~~it is required that~~ the threshold voltages of the cells need to be uniform within the unit cell block.

~~Of them, as the date flash of the flash devices employs a mode~~ When using FN (Fowler-Nordheim) tunneling and not HCE (hot carrier effect) as a program mode, distribution of ~~a~~ the dopant ~~implanted in order~~ to control the threshold voltage becomes an important parameter ~~unlike from the code flash in which formation of the depletion region is important~~. For this reason, it is ~~required~~ important that the distribution of the ion implantation layer ~~be~~ not be changed ~~even in a~~ by the subsequent annealing process ~~within the effective channel length, than~~ so that the operation speed ~~depending on the driving voltage is~~ can be increased by ~~the ion implantation layer for~~ controlling the threshold voltage.

If the isolation film is formed by the SA-STI method, however, a transient enhanced diffusion (TED) of the dopant occurs ~~at~~ during the high temperature oxidization process, which changes the threshold voltage of the device. Furthermore, if ~~a~~ large quantities of dopant ~~of a large mass is~~ are implanted ~~in order~~ to adjust the threshold voltage of the device, ~~fail may happen by means of~~ RDG (remained dopant gettering) ~~that~~ may occur due to the large quantities of dopant used ~~of the large mass~~. RDG can cause device failure. Therefore, in order to minimize damage caused by ion implantation, high temperature annealing must be implemented as a subsequent

process. For this reason, the dopant of the large mass could not which limits the amount of dopant that can be used as an ion for controlling to control the threshold voltage.

In addition, in the case of BF_2 being a dopant that has been which is widely used in order to form a as a dopant when forming shallow effective channel region of a surface channels, dopant loss occurs due to outgasing caused by a the subsequent annealing process. In particular, in the cell necessarily requiring the high temperature process, fluorine-induced (F-induced) F induced outgasing during annealing is inevitable due to maximized outgasing the large quantities of fluorine (F) present and its tendancy to be outgassed. Due to this, there is a problem that the film quality of As a result, the oxide film quality is degraded.

SUMMARY OF THE DISCLOSURE ~~INVENTION~~

Accordingly, the present invention is contrived to substantially obviate one or more problems due to limitations and disadvantages of the related art.

An object of the present invention is to provide a method of manufacturing semiconductor devices is disclosed which is capable of prohibiting by maximum generation of a limiting TED (transient enhanced diffusion) phenomenon of a the dopant and preventing degradation of the oxide film quality due to outgasing, in an during annealing process for thereby mitigating damage or defects caused by ion implantation. In the disclosed process, in a manner that an a monoatomic dopant having a large atomic weight and made of monoatomic is implanted to form an ion implantation layer, instead of using a dopant of a low small atomic weight such as B or a low molecular weight ion such as a BF_2 which has been usually employed, in

~~case that~~ when the ion implantation layer is formed ~~in order~~ to control the threshold voltage of the semiconductor device.

~~Additional advantages, objects, and features of the invention will be set forth in part in the description which follows and in part will become apparent to those having ordinary skill in the art upon examination of the following or may be learned from practice of the invention. The objectives and other advantages of the invention may be realized and attained by the structure particularly pointed out in the written description and claims hereof as well as the appended drawings.~~

~~To achieve these objects and other advantages and in accordance with the purpose of the invention, as embodied and broadly described herein, a~~

A method of manufacturing semiconductor devices according to ~~the present invention is characterized in that it~~ this disclosure comprises ~~the steps of~~ providing a semiconductor substrate for which given processes for forming the semiconductor device ~~are~~ have been implemented, and implanting a ~~3 balance~~ Group III monatomic dopant having a higher atomic weight than boron ~~and made of monoatomic~~ at a given depth of the semiconductor substrate by means of an ion implantation process, thus forming an ion implantation layer.

In the above process, the dopant may be implanted ~~with~~ as a screen oxide film is formed.

The ion implantation process includes implanting ~~a~~ the dopant at a concentration range of ~~5E11 ~ 1E13~~ $5 \times 10^{11} \sim 5 \times 10^{13}$ ion/cm^2 with an energy range of 10 ~ 50KeV. The dopant may be indium. Further, the ion implantation process may include implanting the dopant at a tilt angle of 3 ~ 13°.

Furthermore, a rapid thermal process may be implemented in order to activate the dopant after the ion implantation layer is formed. At this time, the rapid thermal process may be implemented at a temperature range of 800 ~ 1100°C at ~~the ratio~~ a heating rate range of 20 ~ 50°C/sec for time period range of 5 ~ 30 seconds. Also, the ~~raid~~ rapid thermal process may be implemented under a nitrogen atmosphere.

~~In another aspect of the present invention, it is to be understood that both the foregoing general description and the following detailed description of the present invention are exemplary and explanatory and are intended to provide further explanation of the invention as claimed.~~

BRIEF DESCRIPTION OF THE DRAWINGS

The above and other ~~objects,~~ features and advantages of the ~~present invention~~ disclosed process will be apparent from the following detailed description of the preferred embodiments ~~of the invention~~ in conjunction with the accompanying drawings, ~~in which~~ wherein:

FIG. 1A ~ FIG. 1E are cross-sectional views of semiconductor devices for explaining a method of manufacturing the device according to a preferred embodiment ~~of the present invention~~.

DETAILED DESCRIPTION OF THE PRESENTLY PREFERRED EMBODIMENTS

~~Reference will now be made in detail to the preferred embodiments of the present invention, examples of which are illustrated in the accompanying drawings, in which like reference numerals are used to identify the same or similar parts.~~

FIG. 1A ~ FIG. 1E are cross-sectional views of semiconductor devices for explaining a method of manufacturing ~~the~~ semiconductor device according to a preferred embodiment ~~of the present invention~~.

Referring to FIG. 1A, a screen oxide film **102** is formed on a semiconductor substrate **101** as a sacrificial oxide film for crystal defect prohibition or surface treatment of the surface of the semiconductor substrate **101**. The screen oxide film **102** also serves to prohibit inter-diffusion by channeling of the dopant that occurs in the ion implantation process for forming the wells. In ~~the above~~ Fig. 1A, the screen oxide film **102** is formed ~~in~~ using a dry or wet oxidization mode at a temperature range of 750 ~ 800°C and is formed ~~in~~ with a thickness range of 70 ~ 100Å.

Meanwhile, a cleaning process may be implemented before the screen oxide film **102** is formed. At this time, the cleaning process may be implemented by sequentially using hydrofluoric acid (DHF) where H_2O:HF are mixed in ~~the~~ a ratio of 50:1 ~ 100:1 ~~and~~ with a SC-1($NH_4OH/H_2O_2/H_2O$) solution, or sequentially using a BOE (buffered oxide etchant) ~~in which a~~ solution where NH_4F:HF is mixed in ~~the~~ a ratio range of 4:1 ~ 7:1 and is diluted ~~into~~ with H_2O ~~in the~~ to the ratio range of 1:100 ~ 1:300 ~~and~~ in combination with the SC-1($NH_4OH/H_2O_2/H_2O$) solution.

Referring to FIG. 1B, a triple n well **103** is formed on a region where an n channel will be formed by means of the ion implantation process. A p well **104** is consecutively formed in depth shallower than the triple n well **103**. ~~In the above, the~~ The triple n well **103** may be formed by implanting P at a concentration range of ~~5E12 ~ 5E13~~ $5 \times 10^{12} \sim 5 \times 10^{13}$ ion/cm^2 and with an energy range of 500 ~ 2000KeV. The p well **104** may be formed by implanting B at a concentration range of ~~1E12 ~ 5E13~~ $1 \times 10^{12} \sim 5 \times 10^{13}$ ion/cm^2 and with an energy range of 200 ~ 1000KeV. Meanwhile,

an n well (not shown) is formed in another region where a p channel device is to be formed. The n well may be formed by implanting P at a concentration range of ~~1E12 ~ 5E13~~ $1 \times 10^{12} \sim 5 \times 10^{13}$ ion/cm^2 with an energy range of 200 ~ 1000KeV. In the above procedure, it is preferred that the ion implantation process for forming the p well is implemented at a tilt angle range of 3 ~ 13°for the purpose of prohibiting or limiting dopant channeling.

By reference to FIG. 1C, an ion implantation layer **105** for controlling the threshold voltage is formed at a given depth of the p well **104** by means of the ion implantation process in order to control the threshold voltage of the semiconductor device that will be formed ~~in~~ on the semiconductor substrate **101** ~~in a subsequent process~~. ~~In the above, the~~ The ion implantation layer **105** is formed by implanting a monoatomic dopant having a high atomic weight ~~and made of monoatomic~~, instead of using a dopant having a low atomic weight such as B ~~and~~ or a low molecular weight dopant ~~ion~~ such as BF_2 as ~~a dopant that was conventionally used~~ taught by the prior art. For example, the ion implantation layer **105** may be formed by implanting ~~3 balance~~ Group III dopant having a higher atomic weight than boron and ~~made of~~ preferably monoatomic, such as ~~preferably~~ indium although other Group III dopants could be utilized. At this time, the ion implantation process may be implemented using a dopant concentration range of ~~5E11 ~ 1E13~~ $5 \times 10^{11} \sim 1 \times 10^{13}$ ion/cm^2 with an energy range of 10 ~ 50KeV. Meanwhile, like the ion implantation process for forming the p and/or n wells, even when the ion implantation process for controlling the threshold voltage is implemented, it is preferred that ion implantation is implemented at a tilt angle range of 3 ~ 13° in order to ~~prohibit~~ limit dopant channeling of the channel region in a ~~date~~ flash device using a buried channel.

Immediately after the ion implantation layer **105** for controlling the threshold voltage is formed, an annealing process capable of minimizing exposure at high temperature such as RTP (rapid thermal process) is implemented in order to maximize dopant activation. Only activation of the dopant may be maximized while preventing unnecessary rediffusion of the dopant. At this time, the annealing process may be implemented at a temperature range of 800 ~ 1100°C for a time period range of 5 ~ 30 seconds ~~in the~~ at a heating rate range of 20 ~ 50°C /sec. Further, the annealing process may be implemented under a nitrogen atmosphere in order to prevent formation of a native oxide film.

Referring to FIG. 1D, after the screen oxide film (**102** in FIG. 1C) is removed, a gate oxide film (tunnel oxide film **106** in case of ~~the~~ flash devices), a conductive material layer **107** and a pad nitride film **108** are sequentially formed.

In the above, the screen oxide film (**102** in FIG. 1C) is removed by a cleaning process sequentially using hydrofluoric acid (DHF) ~~where~~ with a H_2O:HF ~~is mixed in the~~ ratio of 50:1 ~ 100:1 and SC-1($NH_4OH/H_2O_2/H_2O$) solution.

Thereafter, the gate oxide film **106** is formed by a wet oxidization process at a temperature range of 750 ~ 800°C. The gate oxide film **106** is then annealed under nitrogen atmosphere at a temperature range of 900 ~ 910°C for a time period range of 20 ~ 30minutes in order to minimize an interface defect of the semiconductor substrate **101** and the gate oxide film **106**.

Meanwhile, the conductive material layer **107** may be formed by depositing a doped polysilicon layer the grain size of which is minimized, by means of a LP-CVD (low pressure chemical vapor deposition) method using SiH_4 or Si_2H_6 and PH_3 gas at a temperature range of 580 ~ 620°C under a low pressure range of 0.1 ~ 3 Torr. At this

time, the impurity (P) concentration of the doped polysilicon layer is controlled to ~~be a level~~ a concentration range of ~~1.5E20 ~ 3.0E20~~ $1.5 \times 10^{20} \sim 3.0 \times 10^{20}$ atoms/cc and the doped polysilicon layer is formed in thickness range of 250 ~ 500Å.

The pad nitride film **108** formed on the conductive material layer **107** may be formed in thickness range of 900 ~ 2000Å by means of a ~~the~~ LP-CVD method.

Referring to FIG. 1E, the pad nitride film **108**, the conductive material layer **107** and the gate oxide film **106** in the isolation region are sequentially removed by means of an etch process, thus exposing the semiconductor substrate **101** in the isolation region. Next, the exposed semiconductor substrate **101** in the isolation region is etched by a given depth to form a trench **109**. The trench **109** is then buried with an insulating material (not shown) to form an isolation film (not shown) of a STI (shallow trench isolation) structure (also not shown). In the above, a high density plasma (HDP) oxide film may be used as the insulating material. At this time, the high density plasma (HDP) oxide film is formed in thickness range of 4000 ~ 10000Å on the entire structure so that the trench **109** is completely buried while preventing generating of void spaces.

Although not shown in the drawings, a chemical mechanical polishing process as a subsequent process is ~~continuously implemented~~ carried out so that the insulating material remains only up to a target height rather than the surface of the semiconductor substrate **101** while removing the insulating material on the pad nitride film **108**. Next, after a wet cleaning process using diluted HF is implemented, a conductive material ~~same to~~ like the conductive material **107** is formed in thickness range of 400 ~ 1000Å. A common process of manufacturing ~~the~~ a flash memory cell is implemented to complete the fabrication of the flash memory cell.

As described above, the ~~present invention~~ disclosed methods have ~~has~~ the following benefits ~~effects through the method of manufacturing the semiconductor devices~~:

First, in the memory cell of ~~the date~~ a flash device in which the isolation film of the STI structure requiring ~~frequent~~ one or more high temperature processes ~~must be formed~~, the use of a monoatomic dopant having a high atomic weight ~~and made of monoatomic~~ is implanted to form an ion implantation layer for controlling the threshold voltage. Therefore, the flash device ~~could~~ can be fabricated while minimizing the TED phenomenon.

Second, the uniformity of the threshold voltage ~~could~~ can be secured within the target range while minimizing the TED phenomenon. Therefore, program/erase operation characteristics of a cell block unit ~~could~~ can be improved in the resulting flash memory device.

Third, after the ion implantation layer is formed, there is no outgasing in the ~~course of implementing a~~ subsequent annealing process. It is thus possible to prevent degradation of the film quality of the gate oxide film.

Fourth, it is possible to form ~~the~~ a gate oxide film of a high quality by preventing degradation of the film quality of the gate oxide film caused by the ion implantation processes. Accordingly, it is possible to improve the electrical characteristics and reliability of the ~~date~~ flash memory device using FN tunneling.

Fifth, as dopant damage ~~due to out~~ caused by diffusion is minimized, it is possible to control the threshold voltage with a minimum amount of ion implantation. Furthermore, as generation of ion implantation damage within the channel region is ~~prohibited~~ limited, it is possible to minimize generation of the leakage current.